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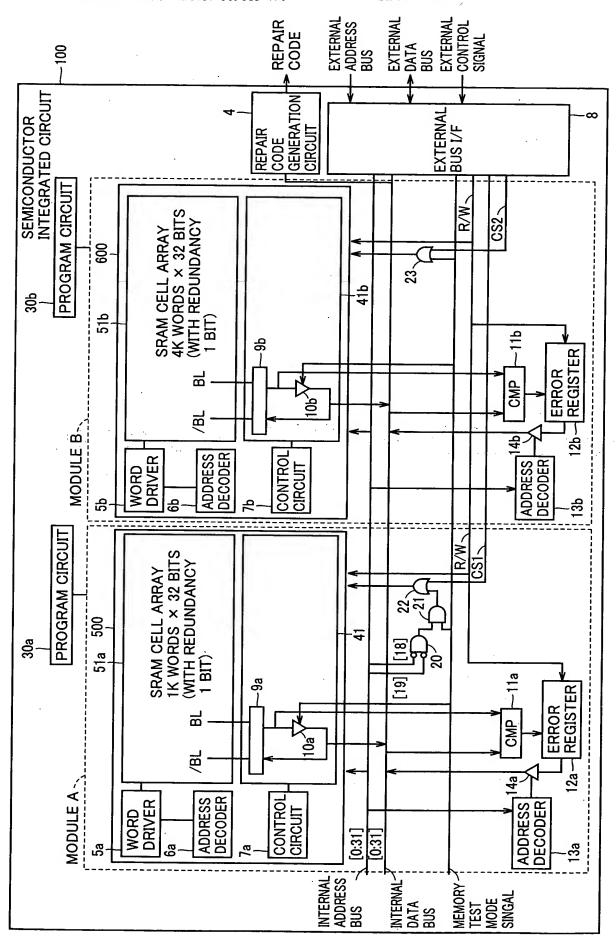
TITLE: SEMICONDUCTOR INTEGRATED CIRCUIT CAPABLE

OF TESTING WITH SMALL SCALE CIRCUIT...

INVENTOR(S): SOICHI KOBAYASHI ET AL.

ATTORNEY DOCKET NO: 009683-476

SHEET 1 of 9



OF TESTING WITH SMALL SCALE CIRCUIT...

INVENTOR(S): SOICHI KOBAYASHI ET AL.

ATTORNEY DOCKET NO: 009683-476

SHEET 2 of 9

FIG.2

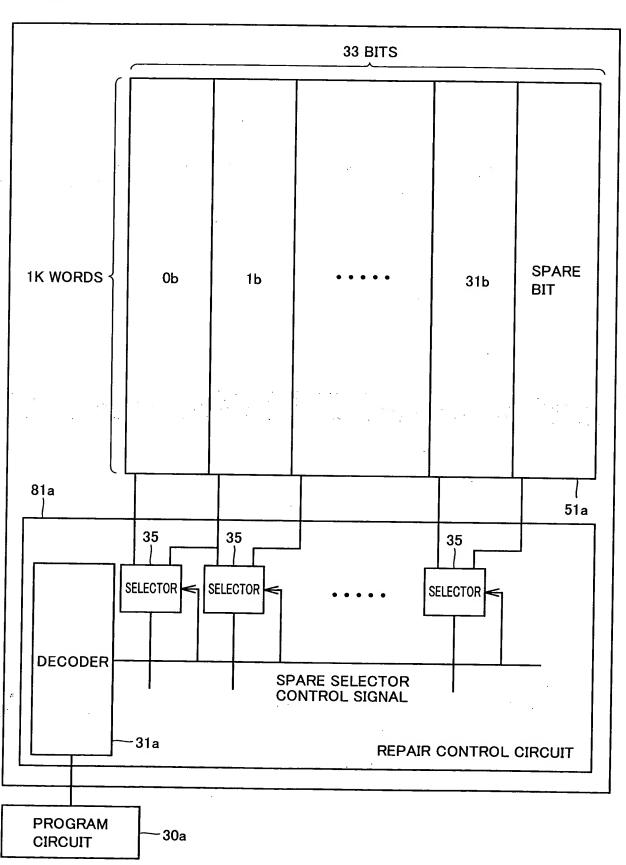
DEFECTIVE	REPAIR CODE						
COLUMN	C0	C1	C2	C3	C4	C5	
NONE	0	0	0	0	0	0	
0	0	0	0	0	0	1	
1	0	0	0	0	1	1	
2	0	0	0	1	0	1	
3	0	0	0	1	1	1	
4	0	0	1	0	0	1	
5	0	0	1	0	1	1	
6	0	0	1	1	0	1	
7	0	0	1	1	1	1	
8	0	1	0	0	0	1	
9	0	1	0	0	1	1	
10	0	1	0	1	0	1	
11	0	1	0	1	1	1	
12	0	1	1	0	0	1	
13	0	1	1	0	1	1	
14	0	. 1	1	1	0	1	
15	0	1.	1	. 1	1 .	1	
16	1	0	0	0	0	1	
17	1	0	0	0	1	1	
18	1	0	0	1	0 .	1	
19	1	0	0	1	1	1	
20	1	0	1	0	0	1	
21	1	0	1	0	1	1	
22	1	0	1	1	0	1	
23	1	0	1	1	1	1	
24	1	1	0	0	0	1	
25	1	1	0	0	1	1	
26	1	1	0	1	0	1	
27	1	1	0	1	1	1	
28	1	1	1	0	0	1	
29	1	1	1	0	1	0	
30	1	1	1	1	0	1	
31	1	1	1	1	1	1	

OF TESTING WITH SMALL SCALE CIRCUIT...

INVENTOR(S): SOICHI KOBAYASHI ET AL. **ATTORNEY DOCKET NO: 009683-476**

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FIG.3



OF TESTING WITH SMALL SCALE CIRCUIT...

INVENTOR(S): SOICHI KOBAYASHI ET AL.

ATTORNEY DOCKET No: 009683-476

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FIG.4

FUSE ELEMENT	REPAIR CODE BIT
F0:NOT-DISCONNECTED	C0=0
F0:DISCONNECTED	C0=1
F1: NOT-DISCONNECTED	C1=0
F1: DISCONNECTED	C1=1
F2: NOT-DISCONNECTED	C2=0
F2: DISCONNECTED	C2=1
F3: NOT-DISCONNECTED	C3=0
F3: DISCONNECTED	C3=1
F4: NOT-DISCONNECTED	C4=0
F4: DISCONNECTED	C4=1
F5:NOT-DISCONNECTED	C5=0
F5:DISCONNECTED	C5=1

OF TESTING WITH SMALL SCALE CIRCUIT...
INVENTOR(S): SOICHI KOBAYASHI ET AL. ATTORNEY DOCKET NO: 009683-476

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FIG.5

FL	JSE	EL		ENT F4		SPARE SELECTOR CONTROL SIGNAL [0:31] (SPARE DECODER OUTPUT VALUE)							
0	0	0	0	0	0	0000	0000	0000	0000	0000	0000	0000	0000
0	0	0	0	0	1	1111	1111	1111	1111	1111	1111	1111	1111
0	0	0	0	1	1	0111	1111	1111	1111	1111	1111	1111	1111
0	0	0	1	0	1	0011	1111	1111	1111	1111	1111	1111	1111
0	0	0	1	1	1	0001	1111	1111	1111	1111	1111	1111	1111
0	0	1	0	0	1	0000	1111	1111	1111	1111	1111	1111	1111
0	0	1	0	1	1	0000	0111	1111	1111	1111	1111	1111	1111
0	0	1	1	0	1	0000	0011	1111	1111	1111	1111	1111	1111
0	0	1	1	1	1	0000	0001	1111	1111	1111	1111	1111	1111
0	1	0	0	0	1	0000	0000	1111	1111	1111	1111	1111	1111
0	1	0	0	1	1	0000	0000	0111	1111	1111	1111	1111	1111
0	1	0	1	0	1	0000	0000	0011	1111	1111	1111	1111	1111
0	1	0	1	1	1	0000	0000	0001	1111	1111	1111	1111	1111
0	1	1	0	0	1	0000	0000	0000	1111	1111	1111	1111	1111
0	1	1	0	1	1	0000	0000	0000	0111	1111	1111	1111	1111
0	1.	_{3.} 1	1	0.	1	0000	0000	0000	0011	1111	1111	1111	1111
0	1	1	1	1	1	0000	0000	0000	0001	1111	1111	1111	1111
1	0	0	0	0	1	0000	0000	0000	0000	1111	1111	1111	1111
1	0	0	0	1	1	0000	0000	0000	0000	0111	1111	1111	1111
1	0	0	1	0	1	0000	0000	0000	0000	0011	1111	1111	1111
1	0	0	1	1	1	0000	0000	0000	0000	0001	1111	1111	1111
1	0	1	0	0	1	0000	0000	0000	0000	0000	1111	1111	1111
1	0	1	0	1	1	0000	0000	0000	0000	0000	0111	1111	1111
1	0	1	1	0	1	0000	0000	0000	0000	0000	0011	1111	1111
1	0	1	1	1	1	0000	0000	0000	0000	0000	0001	1111	1111
1	1	0	0	0	1.	0000	0000	0000	0000	0000	0000	1111	1111
1	1	0	0	1	1	0000	0000	0000	0000	0000	0000	0111	1111
1	1	0	1	0	1	0000	0000	0000	0000	0000	0000	0011	1111
1	1	0	1	1	1	0000	0000	0000	0000	0000	0000	0001	1111
1	1	1	0	0	1	0000	0000	0000	0000	0000	0000	0000	1111
1	1	1	0	1	0	0000	0000	0000	0000	0000	0000	0000	0111
1	1	1	1	0	1	0000	0000	0000	0000	0000	0000	0000	0011
1	1	1	1	1	1	0000	0000	0000	0000	0000	0000	0000	0001

OF TESTING WITH SMALL SCALE CIRCUIT...
INVENTOR(S): SOICHI KOBAYASHI ET AL.

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(2)										(E)
	E2	1000	~	0000			0000			0000
	EI	1000	œ	0000			0000			0000 0000 000
(4)										
				I C						
	8	0000	&	0101	0101	0000	0000	0101	0000	0000
	7	0000	>	0101						
**	9	0000	œ	0101	0101	0000	0000	0101	0000	0000
	22	0000	*	0101						
	4	0000	œ	0101	0101	0000	0000	0101	0000	0000
·	က	0000	>	0101						
	2	0000	В.	0101	0101	0000	0000	0101	0000	0000
	_	0000	×	0101						
	CYCLE	INTERNAL ADDRESS BUS	R/W	INTERNAL DATA BUS	READ DATA FROM SRAM CELL ARRAY 51a IN MODULE A	OUTPUT OF COMPARATOR 11a IN MODULE A	ERROR DATA IN ERROR REGISTER 12a IN MODULE A	READ DATA FROM SRAM CELL ARRAY 51b IN MODULE B	OUTPUT OF COMPARTOR 11b IN MODULE B	ERROR DATA IN ERROR REGISTER 12b IN MODULE B

TITLE: SEMICONDUCTOR INTEGRATED CIRCUIT CAPABLE OF TESTING WITH SMALL SCALE CIRCUIT... INVENTOR(S): SOICHI KOBAYASHI ET AL. ATTORNEY DOCKET NO: 009683-476 SHEET 7 of 9 REPAIR CODE External Address Bus EXTERNAL DATA BUS EXTERNAL CONTROL SIGNAL -200 SEMICONDUCTOR INTEGRATED CIRCUIT REPAIR CODE GENERATION CIRCUIT EXTERNAL BUS I/F ∞ 700 R⁄W ∕ CS3~ PROGRAM CIRCUIT SRAM CELL ARRAY 4K WORDS × 32 BITS (WITH REDUNDANCY 1 BIT) -11b 96 ERROR REGISTER 필 CMP 9 BL 12b-14p BANK B 43b DECODER ADDRESS 85b 13b 53b-CONTROL CIRCUIT WORD DRIVER 93 88b ADDRESS DECODER 92. 85a 87 WORD DRIVER 7 88a 91 CONTROL -30a CIRCUIT 53a 90 PROGRAM CIRCUIT SRAM CELL ARRAY
4K WORDS × 32 BITS
(WITH REDUNDANCY
1 BIT) REGISTER BE ERROR CMP 10aBL 12a-BANK A MODULE C 43a DECODER ADDRESS [0:31] [0.31]13a INTERNAL ADDRESS INTERNAL MEMORY -TEST Mode Singal DATA BUS BUS

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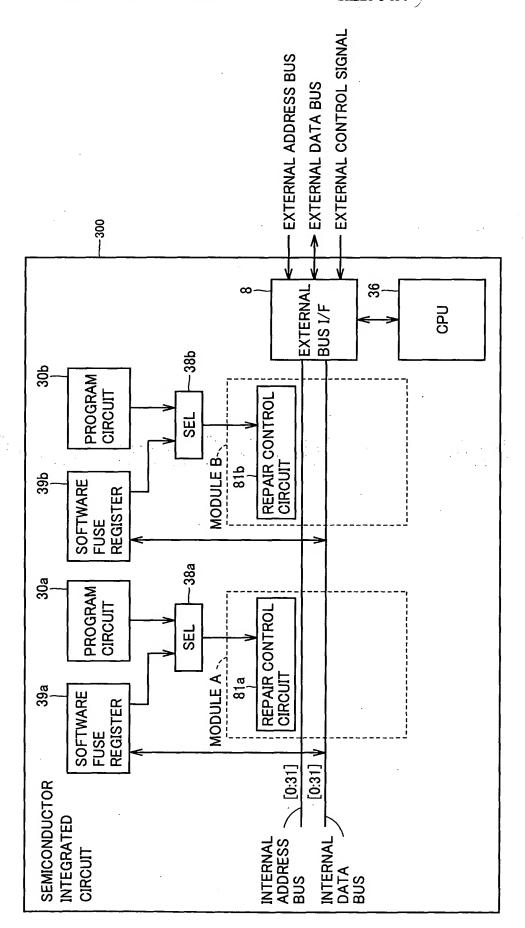
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FIG.9

